REMARKS/ARGUMENT

Claims 1-7 are pending in this application. Claims 1-7 stand rejected. In light of the remarks set forth below, Applicant respectfully submits that each of the pending claims is in immediate condition for allowance.

Claims 1 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,351,458 ("Miya") in view of U.S. Patent No. 5,375,146 ("Chalmers"). Applicant requests withdrawal of this rejection.

Among the limitations of independent claims 1 and 5 neither shown nor suggested in Miya is a "pilot symbol, contained only in a received signal."

The Office Action states that "Miya discloses an interpolation-type synchronous detection system (col. 3, lns. 1-19). Pilot symbols are periodically interpolated in information signals to be transmitted, the transfer function is estimated and detection is carried out." (Office Action at 2). However, this portion of Miya is explicitly referring to the prior art of Higashi which was distinguished in Applicant's previous response. The Examiner recognized that Applicant distinguished the Higashi reference with the withdrawal of the rejection in light of Higashi. Thus, the Miya reference should be withdrawn as well.

Applicant disagrees that Miya discloses the pilot symbol, contained only in a received signal as explicitly recited in Applicant's claim. In Miya, the pilot symbols are periodically interpolated in information symbols as shown in Figure 11. Miya only discloses

pilot symbols that are periodically interpolated in information signals to be transmitted. Thus, claims 1 and 5 are allowable over the cited references.

Further, Chalmers merely discloses that, with respect to individual data symbols, it is possible to adopt a reception sampling point to optimize an eye pattern of each data symbol as a sampling point. In contrast, in the present invention, each data symbol is sandwiched between pilot symbols, thereby making it possible to optimize the update timing of the reception sampling point which is subject to oversampling. The claimed interpolation synchronous detection method optimizes the updating timing of the reception sampling point of each data symbol. Accordingly, transmission error (phase error) can be minimized by changing the transfer functions at the middle time point between pilot symbols sandwiching the data symbol. The transmission error is, in fact, caused by the oversampling point with respect to the pilot symbols sandwiching the data symbol is different. Thus, claims 1 and 5 are allowable over the cited references.

Claims 2, 4 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Miya in view of U.S Patent No. 6,178,194 ("Yamada") further in view of Chalmers. Applicant requests withdrawal of this rejection. Miya discloses pilot symbols that are periodically interpolated in information signals to be transmitted. As discussed above, Miya fails to disclose a method or system having a pilot symbol contained only in a received signal. The addition of Yamada or Chalmers fails to cure this deficiency. Thus, claims 2, 4 and 7 are allowable over the cited references.

Claims 1, 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,178,194 ("Vasic") in view of Chalmers. Applicant requests withdrawal of this rejection. The Office Action states that "Vasic does not disclose updating a middle point of the data frame at reception sampling point." The Office Action then attempts to cure this deficiency with Chalmers, which discloses a circuit that shifts the sample timing phase so that the sampling occurs at the maximum opening of the receiver eye pattern (i.e., sampling in the middle of a digital symbol). In Chalmers, a digital down conversion process is disclosed where symbol timing correction, under control of a DSP demodulator's timing recovery loop can be performed digitally.

> In conventional demodulators, the A/D sample clock is steered by a timing correction circuit which is driven by the demodulator's timing recovery loop. The circuit shifts the sample timing phase so that the sampling occurs at the maximum opening of the receiver eye pattern (i.e., sampling the middle of a digital symbol) to minimize inter-symbol interference. However, in the inventive digital down converter, the A/D sample clock is free running.

(Chalmers col. 13, lns. 15-25). Thus, Chalmers teaches away from sampling occurring at a fixed point. In Chalmers, the sample clock is free running. Thus, because Chalmers actually teaches away from using a sampling circuit that samples at the maximum opening of the receiver eye pattern, one would not combine Chalmers and Miya. Thus, claims 1, 5 and 6 are allowable over the cited references.

Claims 2, 4 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Vasic in view of Yamada further in view of Chalmers. Applicant requests withdrawal of this rejection. As discussed above, Chalmers actually teaches away from a fixed sampling in the

middle of a digital symbol but uses a free running sample clock. Thus, Applicant respectfully requests withdrawal of this rejection.

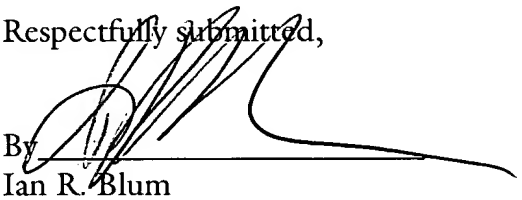
Applicant has responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

The amendments to the claims are for clarification purposes only and are not intended to limit the scope of the claims in any way. It is asserted that the present amendment places the application in a form for allowance. Entry of this amendment is therefore earnestly solicited.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: June 30, 2003

Respectfully submitted,



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